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ABSTRACT OF THE DISCLOSURE

Systems and methods are described for a core sync module. A method includes receiving a pair of input clock signals; utilizing a stratum clock state machine to control a multiplexer; utilizing the multiplexer to switch an input of a main clock between each of the pair of input clock signals; inducing a phase build-out activity; and transmitting an output clock signal. An apparatus includes a first input clock digital phase-locked loop; a second input clock digital phase-locked loop; a stratum clock state machine coupled to the first input clock digital phase-locked loop and to the second input clock digital phase-locked loop; and a main clock phase-locked loop coupled to the first input clock digital phase-locked loop, to the second input clock digital phase-locked and to the stratum clock state machine.